IN THE CLAIMS

Claims 1-29 (Canceled).

Claim 30 (Currently Amended): A method of manufacturing a semiconductor memory, comprising;

forming a transistor including a first impurity-diffused region, a second impurity-diffused region, and a gate between the first impurity-diffused region and the second impurity-diffused region on the semiconductor substrate;

forming a lower electrode layer over the transistor, and being connected to the first impurity-diffused region;

forming a ferroelectric layer on the lower electrode;

forming an upper electrode layer on the ferroelectric layer;

forming the upper electrode layer into a first upper electrode and a second upper electrode;

forming the lower electrode layer and the ferroelectric layer into a capacitor shape;

forming a wiring layer connecting between the first upper electrode and the second impurity-diffused region;

covering the ~~semiconductor substrate, the transistor, the lower electrode, the ferroelectric layer, the wiring layer, the first upper electrode, and the~~ second upper electrode with insulating layer ~~to insulate~~, such that the second upper electrode is insulated from the ~~other except~~ first and second impurity-diffused regions by the insulating layer and the ferroelectric layer.

Claim 31 (Currently Amended): A manufacturing method of semiconductor memory, comprising;

forming a cell transistor including a first impurity diffused region, a second impurity-diffused region, and a gate between the first impurity-diffused region and the second impurity-diffused region on the semiconductor substrate;

forming a block selecting transistor including a third impurity diffused-region, a fourth impurity-diffused region, and a gate between the third impurity-diffused region and the fourth impurity-diffused region on the semiconductor substrate, and being adjoined to the cell transistor;

forming a lower electrode layer over the cell transistor and the block selecting transistor, and being connected to the first impurity-diffused region;

forming a ferroelectric layer on the lower electrode;

forming an upper electrode layer on the ferroelectric layer;

forming the upper electrode layer into a first upper electrode and a second upper electrode;

forming the lower electrode layer and the ferroelectric layer into a capacitor shape;

forming a wiring layer connecting between the first upper electrode and the second impurity-diffused region; and

covering the ~~semiconductor substrate, the cell transistor, the block selecting transistor, the lower electrode, the ferroelectric layer, the wiring layer, the first upper electrode, and the~~ second upper electrode with insulating layer ~~to insulate~~, such that the second upper electrode is insulated from the ~~other except~~ first and second impurity-diffused regions by the insulating layer and the ferroelectric layer.